REMARKS

The following remarks are provided in response to the Office Action mailed October 11, 2006, in which the Examiner:

- rejected claims 35-50 under 35 U.S.C. §103(a) as being unpatentable over U.S. 2003/0132466 to Shin et al. (hereinafter Shin) in view of JP 05226361 to Matshuhashi (hereinafter Matsuhashi) and WO 00/77828 to Stolk et al. (hereinafter Stolk).

The applicants respectfully request reconsideration of the above referenced patent application for the following reasons:

Claims 35-50 rejection under 35 U.S.C. §103(a)

Claims 35-50 are rejected under 35 U.S.C. §103(a) as being unpatentable over Shin in view of Matsuhashi and Stolk. The Applicants herein cancel claims 41 and 49 without prejudice. The Applicants herein amend independent claims 35 and 43, from which claims 36-40, 42, 44-48 and 50 depend, and respectfully request that the Examiner reconsider claims 35-40, 42-48 and 50 in light of the amendments and the following arguments.

In claims 35-50, the Applicants teach and claim a transistor comprising a dielectric layer above a substrate and a trench in the dielectric layer, wherein the bottom of the trench is directly above the substrate. A gate dielectric layer is in the trench and a first portion of the gate dielectric layer is adjacent to a first sidewall of the trench, a second portion of the gate dielectric layer is adjacent to a second sidewall of the trench

and a third portion of the gate dielectric layer is on the bottom of the trench. A gate electrode in the trench and is directly between the first and second portions of the gate dielectric layer. The gate electrode is comprised of a central portion and a pair of outer portions, wherein the outer portions are each comprised of a sidewall region and an extension region. The central portion is directly adjacent to the sidewall region and directly above the extension region of each of the outer portions. The bottom surfaces of the central portion and the pair of outer portions of the gate electrode are directly on the third portion of the gate dielectric layer. The workfunction of the pair of outer portions is different than the workfunction of the central portion. Finally, a pair of source/drain regions is in the substrate on opposite sides of the pair of outer portions of the gate electrode. That is, the applicants teach and claim a transistor having **a gate electrode comprising a pair of outer portions, wherein each outer portion comprises a sidewall region and an extension region** (outer portion with sidewall region and extension region: *see* item "222" of Fig. 2, item "322" of Figs. 3G-3K, and paragraphs [0011] and [0026]).

In claims 35-42, the transistor is an NMOS transistor, the workfunction of said pair of outer portions is lower than the workfunction of said central portion, and the pair of source/drain regions is a pair of n type source/drain regions. In claims 43-50, the transistor is a PMOS transistor, the workfunction of said pair of outer portions is higher than the workfunction of said central portion, and the pair of source/drain regions is a pair of p type source/drain regions.

None of Shin, Matshuhashi nor Stolk disclose a transistor having a gate electrode comprising a pair of outer portions, wherein each outer portion comprises a sidewall region and an extension region, as taught by the Applicants. All three references do disclose a transistor having three portions of a gate electrode. However, the outer regions of the gate electrodes of Shin, Matshuhashi and Stolk are fabricated by an anisotropic etch process and therefore only comprise sidewall regions. The Applicants teach fabricating outer regions of a gate electrode by angled deposition, thus forming both sidewall and extension regions for each outer portion of the gate electrode. Thus, **Shin, Matshuhashi and Stolk disclose a gate electrode having outer portions comprised of only a sidewall region**, whereas **the Applicants teach a gate electrode having outer portions comprised of both a sidewall region and an extension region.**

New Claims 51-70

New claims 51 – 62 are dependent upon currently amended independent claims 35 and 43. In light of the amendments to claims 35 and 43, the Applicants respectfully request consideration of the new claims 51 – 62.

In new claims 63 – 70, the Applicants teach and claim a transistor comprising a dielectric layer above a substrate and a trench in the dielectric layer, wherein the bottom of the trench is directly above the substrate. A gate dielectric layer is on the bottom of the trench. A gate electrode in the trench is comprised of a central portion and a pair of outer portions, wherein the outer portions are each comprised of a sidewall region and an extension region. The central portion is directly adjacent to the sidewall region and

directly above the extension region of each of the outer portions. The workfunction of the pair of outer portions is different than the workfunction of the central portion. Finally, a pair of source/drain regions is in the substrate on opposite sides of the pair of outer portions of the gate electrode. That is, the applicants teach and claim a transistor having **a gate electrode comprising a pair of outer portions, wherein each outer portion comprises a sidewall region and an extension region** (outer portion with sidewall region and extension region: *see* item "222" of Fig. 2, item "322" of Figs. 3G-3K, and paragraphs [0011] and [0026]).

None of Shin, Matshuhashi nor Stolk disclose a transistor having a gate electrode comprising a pair of outer portions, wherein each outer portion comprises a sidewall region and an extension region, as taught by the Applicants. All three references do disclose a transistor having three portions of a gate electrode. However, the outer regions of the gate electrodes of Shin, Matshuhashi and Stolk are fabricated by an anisotropic etch process and therefore only comprise sidewall regions. The Applicants teach fabricating outer regions of a gate electrode by angled deposition, thus forming both sidewall and extension regions for each outer portion of the gate electrode. Thus, **Shin, Matshuhashi and Stolk disclose a gate electrode having outer portions comprised of only a sidewall region**, whereas **the Applicants teach a gate electrode having outer portions comprised of both a sidewall region and an extension region**.

CONCLUSION

The Applicants submit that they have overcome the Examiner's rejections of the claims and that they have the right to claim the invention as set forth in the listed claims. The Examiner is respectfully requested to contact the undersigned by telephone if it is believed that such contact would further the examination of the present application.

Pursuant to 37 C.F.R. 1.136(a)(3), applicant(s) hereby request and authorize the U.S. Patent and Trademark Office to (1) treat any concurrent or future reply that requires a petition for extension of time as incorporating a petition for extension of time for the appropriate length of time and (2) charge all required fees, including extension of time fees and fees under 37 C.F.R. 1.16 and 1.17, to Deposit Account No. 02-2666.

Respectfully submitted,

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Dated

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